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## (54) SILICON SINGLE CRYSTAL INGOT AND SILICON WAFER MADE OF THE SAME

### (57)Abstract:

**PROBLEM TO BE SOLVED:** To obtain a single crystal ingot and wafer excellent in electrical characteristics by suppressing the formation of agglomerate of hole-type point defects and interstitial silicon-type point defects and lowering the contamination concentration of iron to be not more than a specific value in a Czochralski method.

**SOLUTION:** Silicon molten liquid is obtained by washing, preferably at least two times, source silicon with an aqueous solution containing dissolved ozone and then hydrofluoric acid or nitrohydrofluoric acid, and, after finally washing with ultra-pure water, melting the source silicon in a furnace based on a Czochralski method. The ratio of solidification is preferably set to be not less than 0.9 at initial pulling-up and the ratio of solidification is set to be not more than 0.9, preferably not more than 0.8 when the single crystal is pulled up after remelting. Thereby, the contamination concentration of iron element becomes not more than  $2 \times 10^9$  atoms/cm<sup>3</sup>. When the rate of pulling-up an ingot is set as V (mm/min) and the temp. gradient at the interface between the ingot and the silicon molten liquid is set to be G (°C/mm), the value of V/G (mm<sup>2</sup>/min.°C) is determined over whole length of the ingot by simulation, and the ingot is grown, thereby a crystal free from defects can be obtained.

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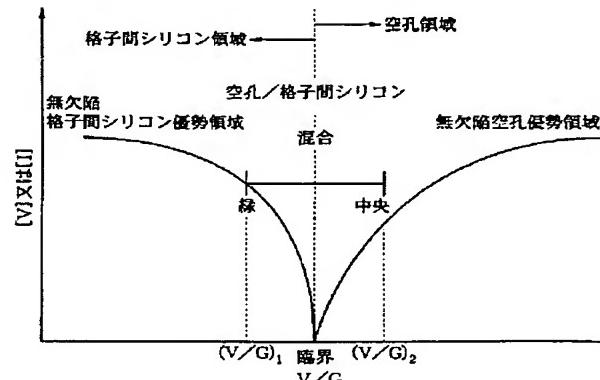
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(54) 【発明の名称】 シリコン単結晶インゴット及びこれから作られたシリコンウェーハ

(57) 【要約】

【課題】 結晶に起因した欠陥がなく、かつ鉄元素のような金属元素の汚染度が小さく電気的特性に優れる。

【解決手段】 C Z 法により育成された空孔型点欠陥の凝集体及び格子間シリコン点欠陥の凝集体が存在しないシリコン単結晶インゴットであって、鉄汚染濃度が  $2 \times 10^9 \text{ atoms/cm}^3$  以下であることを特徴とするシリコン単結晶インゴットである。



## 【特許請求の範囲】

【請求項1】 空孔型点欠陥の凝集体及び格子間シリコン型点欠陥の凝集体が存在しないチョクラルスキー法により育成されたシリコン単結晶インゴットであって、鉄汚染濃度が $2 \times 10^9$  atoms/cm<sup>3</sup>以下であることを特徴とするシリコン単結晶インゴット。

【請求項2】 請求項1記載のシリコン単結晶インゴットから作られたシリコンウェーハ。

## 【発明の詳細な説明】

## 【0001】

【発明の属する技術分野】本発明は、チョクラルスキー法(以下、CZ法といふ。)により育成されたシリコン単結晶インゴット及びこれから作られたシリコンウェーハに関するものである。

## 【0002】

【従来の技術】LSI等の半導体装置は、pn接合においてリーク電流が少なく、またMOSトランジスタのゲート酸化膜に対する信頼性が高い等の優れた電気的特性を示すことが要求される。これらの特性を劣化させる原因として、基板となるシリコンウェーハの結晶欠陥、及びウェーハの金属元素による汚染が挙げられる。金属の中でも特に鉄元素がシリコン単結晶中で強く悪影響を及ぼすとされており、この鉄元素は周囲の環境或いは装置からの汚染により取込まれる。

【0003】このシリコンウェーハの動作領域から鉄元素のような金属元素を捕獲する技術として、従来からウェーハ自体に金属元素を捕獲するゲッタリング能力を持たせるイントリンシックゲッタリング(IG)法や、エクストリンシックゲッタリング(EG)法が知られている。また動作領域となるウェーハ表面から金属を除去する技術として、シリコンウェーハを過酸化水素と水酸化アンモニウムからなるSC-1溶液により洗浄した後、過酸化水素と希塗酸からなるSC-2溶液により洗浄するRCA洗浄法が知られている。

## 【0004】

【発明が解決しようとする課題】しかし、CZ法で育成したシリコン単結晶インゴットに金属元素が多く混入していると、シリコンウェーハの状態での金属元素を除去又は捕獲する技術をますます複雑化又は高度化しなければならない。本発明の目的は、結晶に起因した欠陥がなく、かつ鉄元素のような金属元素の汚染度が小さく電気的特性に優れたシリコン単結晶インゴット及びこれから作られたシリコンウェーハを提供することにある。

## 【0005】

【課題を解決するための手段】請求項1に係る発明は、チョクラルスキー法により育成された空孔型点欠陥の凝集体及び格子間シリコン点欠陥の凝集体が存在しないシリコン単結晶インゴットであって、鉄汚染濃度が $2 \times 1$

$0^9$  atoms/cm<sup>3</sup>以下であることを特徴とするシリコン単結晶インゴットである。請求項2に係る発明は、請求項1記載のシリコン単結晶インゴットから作られたシリコンウェーハである。請求項1に係るインゴット又は請求項2に係るシリコンウェーハは、結晶に起因した欠陥がなく、かつ鉄汚染濃度が $2 \times 10^9$  atoms/cm<sup>3</sup>以下と低いため、LSI等の半導体装置にしたときに、pn接合においてリーク電流が少なく、またMOSトランジスタのゲート酸化膜に対する信頼性が高い等の優れた電気的特性を示す。

## 【0006】

【発明の実施の形態】本発明のシリコン単結晶インゴットを金属元素の含有量を少なくして、かつ無欠陥で製造する方法について述べる。

## (1) 金属元素の含有量の少ないシリコン単結晶の製造方法

本発明の金属元素、特に鉄元素の含有量の少ないシリコン単結晶インゴットは、原料となる塊状又は粒状の多結晶シリコンを洗浄する工程と、洗浄した原料シリコンを融解してこのシリコン融液からCZ法により固化率0.9以下でシリコン単結晶インゴットを育成するシリコン単結晶の引上げ工程と、この引上げたシリコン単結晶を塊状又は粒状にする工程と、この塊状又は粒状の単結晶シリコンを洗浄する工程と、洗浄したシリコン単結晶を再度融解(リメルト)して固化率0.9以下で育成するシリコン単結晶の再引上げ工程とを含む。ここで固化率とは重量換算で原料シリコン100%に対して、育成したシリコン単結晶の割合をいう。

【0007】原料シリコンとなる多結晶シリコン又は単結晶シリコンを洗浄するには、先ず塊状又は粒状の原料シリコンを溶存オゾン水溶液で洗浄した後、フッ酸又はフッ硝酸(フッ酸と硝酸の混酸)で洗浄し、更に超純水で洗浄する方法である。このフッ酸又はフッ硝酸による洗浄工程を1回以上繰返すか、或いは溶存オゾン水溶液による洗浄工程と、フッ酸又はフッ硝酸による洗浄工程を1回以上繰返すことが好ましい。多結晶シリコン又は単結晶シリコンなどの原料シリコンは活性な性質を有するため、石英るつぼに投入するまで、プラスチック製の袋に入れられ密封される。しかし密封の前後において、

空気中の酸素と反応して原料シリコンの表面には酸化膜が形成され易い。この酸化膜は原料シリコンの表面に付着している金属不純物等を含んで形成されたり、或いは酸化膜の形成後に酸化膜の表面に金属不純物等が付着したりする。上記方法において、溶存オゾン水溶液の洗浄によりシリコン表面が強制的に酸化されてシリコン全面に酸化膜が形成され、次いでフッ酸又はフッ硝酸の洗浄によりこの酸化膜が除去される。この結果、酸化膜に含まれる金属不純物等が酸化膜とともに除去される。フッ酸又はフッ硝酸による洗浄工程を1回以上繰返すことにより、その除去効果が高まる。

【0008】上記洗浄で得られた原料シリコンは、CZ法に基づく炉で融解されシリコン融液となる。ここで最初の引上げ時の固化率は0.9以上に、またリメルト後の引上げ時の固化率は0.9以下、好ましくは0.8以下に設定する。固化率を上記値以下にするのは次の理由による。固化率が小さく、石英るっぽ内のシリコン融液が多量に残留しているときの育成された部分、即ちインゴットのトップ部に近い部分は、シリコン融液中の鉄などの金属元素の混入量は少ない。その反面、石英るっぽ内のシリコン融液の残液が少なくなつて固化率が大きくなるに従って、残液中の金属元素の濃度は高くなり、金属元素のインゴットへの混入量が多くなるためである。原料シリコンの洗浄と所定の固化率以下のリメルトにより、シリコン単結晶中の鉄汚染濃度は $2 \times 10^3$  ato m s / cm<sup>3</sup>以下となる。

【0009】(2) 無欠陥シリコン単結晶の製造方法  
次に空孔型点欠陥の凝集体及び格子間シリコン型点欠陥の凝集体が存在しない無欠陥シリコン単結晶の製造方法について述べる。本発明のシリコン単結晶インゴットは、CZ法によりホットゾーン炉内のシリコン融液からインゴットをボロンコフ(Voronkov)の理論に基づいた所定の引上げ速度プロファイルで引上げられる。また本発明のシリコンウェーハはこのインゴットをスライスして作製される。一般的に、CZ法によりホットゾーン炉内のシリコン融液からシリコン単結晶のインゴットを引上げたときには、シリコン単結晶における欠陥として、点欠陥(point defect)と点欠陥の凝集体(agglomerates:三次元欠陥)が発生する。点欠陥は空孔型点欠陥と格子間シリコン型点欠陥という二つの一般的な形態がある。空孔型点欠陥は一つのシリコン原子がシリコン結晶格子で正常的な位置の一つから離脱したものである。このような空孔が空孔型点欠陥になる。一方、原子がシリコン結晶の格子点以外の位置(インターチャンクルサイト)で発見されるとこれが格子間シリコン点欠陥になる。

【0010】点欠陥は一般的にシリコン融液(溶融シリコン)とインゴット(固状シリコン)の間の接触面で形成される。しかし、インゴットを継続的に引上げることによって接触面であった部分は引上げとともに冷却し始める。冷却の間、空孔型点欠陥又は格子間シリコン型点欠陥は拡散により互いに合併して、空孔型点欠陥の凝集体(vacancy agglomerates)又は格子間シリコン型点欠陥の凝集体(interstitial agglomerates)が形成される。言い換れば、凝集体は点欠陥の合併に起因して発生する三次元構造である。空孔型点欠陥の凝集体はCOP(Crystal Originated Particle)、LSTD(Laser Scattering Tomograph Defects)又はFPD(Flow Pattern Defects)と呼ばれる欠陥を含み、格子間シリコン型点欠陥の凝集体はLD(Interstitial-type Large Dislocation)と呼ばれる欠陥を含む。ここでCOP

は鏡面研磨後のシリコンウェーハをアンモニアと過酸化水素の混合液で洗浄すると、ウェーハ表面にビットが形成され、このウェーハをパーティクルカウンタで測定すると、ビットも本来のパーティクルとともにパーティクルとして検出される結晶に起因した欠陥である。FPDとは、インゴットをスライスして作製されたシリコンウェーハを30分間セコ(Secco)エッティング液で化学エッティングしたときに現れる特異なフローパターンを呈する痕跡の源であり、LSTDとは、シリコン単結晶内に赤外線を照射したときにシリコンとは異なる屈折率を有し散乱光を発生する源である。LDは、転位クラスターとも呼ばれたり、或いはこの欠陥を生じたシリコンウェーハをフッ酸を主成分とする選択エッティング液に浸漬するとビットを生じることから転位ビットとも呼ばれる。

【0011】ボロンコフの理論は、欠陥の数が少ない高純度インゴットを成長させるために、インゴットの引上げ速度をV(mm/min)、ホットゾーン構造でインゴットシリコン融液の接触面の温度勾配をG(°C/mm)とするときに、V/G(mm<sup>2</sup>/min·°C)を制御することである。この理論では、図1に示すように、V/Gは関数として空孔濃度及び格子間シリコン濃度を式的に表現し、ウェーハで空孔/格子間シリコン領域の境界がV/Gによって決定されることを説明している。より詳しくは、V/G比が臨界点以上では空孔型点欠陥が支配的に存在するインゴットが形成される反面、V/G比が臨界点以下では格子間シリコン型点欠陥が支配的に存在するインゴットが形成される。

【0012】本発明の所定の引上げ速度プロファイルは、インゴットがホットゾーン炉内のシリコン融液から引上げられる時、温度勾配に対する引上げ速度の比(V/G)が格子間シリコン型点欠陥の凝集体の発生を防止する第1臨界比((V/G)<sub>1</sub>)以上であって、空孔型点欠陥の凝集体をインゴットの中央にある空孔型点欠陥が支配的に存在する領域内に制限する第2臨界比((V/G)<sub>2</sub>)以下に維持されるように決められる。この引上げ速度のプロファイルは、実験的に基準インゴットを軸方向にスライスすることで、実験的に基準インゴットをウェーハにスライスすることで、またはこれらの技術を組合わせることで、シミュレーションによって上記ボロンコフの理論に基づき決定される。即ち、この決定は、シミュレーションの後、インゴットの軸方向スライス及びスライスされたウェーハの確認を行い、更にシミュレーションを繰り返すことによりなされる。シミュレーションのために複数種類の引上げ速度が所定の範囲で決められ、複数個の基準インゴットが成長される。図2に示すように、シミュレーションのための引上げ速度プロファイルは1.2mm/minのような高い引上げ速度(a)から0.5mm/minの低い引上げ速度(c)及び再び高い引上げ速度(d)に調整される。上記低い引上げ速度は0.4mm/min又はそれ以下であることもあって

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もよく、引上げ速度（b）及び（d）での変化は線形的なものが望ましい。

【0013】異なった速度で引上げられ複数個の基準インゴットは各別に軸方向にスライスされる。最適のV/Gが軸方向のスライス、ウェーハの確認及びシミュレーションの結果の相関関係から決定され、続いて最適な引上げ速度プロファイルが決定され、そのプロファイルでインゴットが製造される。実際の引上げ速度プロファイルは所望のインゴットの直径、使用される特定のホットゾーン炉及びシリコン融液の品質等を含めてこれに限定されない多くの変数に依存する。

【0014】図3はシミュレーションと実験的な技術の結合を利用して決定された100cmの長さと200mmの直径を有するインゴットを成長させるための引上げ速度のプロファイルを示す。ここでは三菱マテリアルシリコン（株）生野工場で製作されたモデル名Q41のCZ法に基づいたホットゾーン炉が使用された。

【0015】引上げ速度を徐々に低下させてV/Gを連続的に低下させ、再び引上げ速度を徐々に高めてV/Gを連続的に高めたときのインゴットの断面図を描いてみると、図4に示される事実が分かる。図4には、インゴット内での空孔型点欠陥が支配的に存在する領域が[V]、格子間シリコン型点欠陥が支配的に存在する領域が[P]、及び空孔型点欠陥の凝集体及び格子間シリコン型点欠陥の凝集体が存在しないバーフェクト領域が[P']としてそれぞれ示される。図4に示すように、インゴットの軸方向位置P<sub>1</sub>及びP<sub>2</sub>は、中央に空孔型点欠陥が支配的に存在する領域を含む。位置P<sub>3</sub>及びP<sub>4</sub>は格子間シリコン型点欠陥が支配的に存在するリング及び中央のバーフェクト領域を含む。また位置P<sub>5</sub>及びP<sub>6</sub>は中央に空孔型点欠陥がないし縁部分に格子間シリコン型点欠陥もないので全てバーフェクト領域である。

【0016】図4から明らかのように、複数個の位置P<sub>1</sub>及びP<sub>2</sub>にそれぞれ対応したウェーハW<sub>1</sub>及びW<sub>2</sub>は、中央に空孔型点欠陥が支配的に存在する領域を含む。ウェーハW<sub>3</sub>及びW<sub>4</sub>は格子間シリコン型点欠陥が支配的に存在するリング及び中央のバーフェクト領域を含む。またウェーハW<sub>5</sub>及びW<sub>6</sub>は中央に空孔型点欠陥がないし縁部分に格子間シリコン型点欠陥もないので全てバーフェクト領域である。ウェーハW<sub>7</sub>及びW<sub>8</sub>は、図5に示すように全てバーフェクト領域を作るよう選定して決められた引上げ速度プロファイルで成長したインゴットをスライスして作製される。図6はその平面図である。参考までに、別の引上げ速度プロファイルで成長したインゴットをスライスして作製されたウェーハW<sub>9</sub>及びW<sub>10</sub>が図7に示される。図8はその平面図である。本発明のシリコンウェーハは、上記ウェーハW<sub>1</sub>又はW<sub>2</sub>であって、このウェーハをラッピングし、面取り加工を施した後、鏡面研磨して得られる。

## 【0017】

【実施例】次に本発明の実施例を説明する。原料となる多結晶シリコンの鉄元素濃度をICP質量分析計(inductively coupled plasma mass spectrometer)で測定したところ、平均値が2ppb-wtであった。鉄元素の濃度が2ppb-wtであるということは、シリコン1gに対して鉄が2ppbの割合で含まれていることを意味する。一般に、シリコン単結晶中の不純物濃度は、偏析のため極端に小さく、直接分析するのは困難な元素が多い。そこで、CZ法で単結晶を育成した後、るつぼ内に残ったシリコン融液（以下、残湯という。）を分析し、各不純物元素の偏析係数から、結晶中の不純物濃度を算出する方法が採られる。この分析は通常残湯の一部をサンプリングして固化させた後にこのサンプル全量を高純度なフッ酸と硝酸の混酸により溶解し、ICP質量分析計で分析する。

【0018】この実施例では、あらかじめ多結晶シリコンを融解したシリコン融液の残湯分析とシリコン単結晶のリメルト試験を行って、金属不純物のうち、鉄とクロムとニッケルの濃度について考察した。即ち、上記多結晶シリコンを融解したシリコン融液から単結晶を220mmの長さまで引上げた。固化率0.626のときの残湯をサンプリングして固化し、鉄、クロム及びニッケルの各元素の濃度を測定した。また単結晶のトップ部の鉄、クロム及びニッケルの各元素の濃度も測定した。次いで育成したシリコン単結晶を再度融解（リメルト）して、このシリコン融液から単結晶をやはり220mmの長さまで引上げた。固化率0.681のときの残湯をサンプリングして固化し、鉄、クロム及びニッケルの各元素の濃度を測定した。また単結晶のトップ部の鉄、クロム及びニッケルの各元素の濃度も測定した。

【0019】上記最初のシリコン融液及び再度融解したシリコン融液から引上げたそれぞれの単結晶のトップ部の不純物濃度は、結晶育成前に全ての不純物がシリコン融液中に混入していると仮定し、次の式（1）を用いて計算した。

## 【0020】

## 【数1】

$$C_T = \frac{k_z C_z}{(1-L)^{k_{z-1}}} \dots \quad (1)$$

【0021】但し、C<sub>T</sub>はトップ部の不純物濃度、k<sub>z</sub>は偏析係数、C<sub>z</sub>は残湯中の不純物濃度、Lは残湯分析時の固化率である。鉄元素の偏析係数は $8 \times 10^{-6}$ 、クロム元素の偏析係数は $2 \cdot 8 \times 10^{-5}$ 、ニッケル元素の偏析係数は $3 \times 10^{-5}$ である。残湯中の不純物濃度、トップ部の不純物濃度等の結果を表1に示す。

## 【0022】

## 【表1】

		多結晶シリコン	単結晶リメルト (固化率0.9以下)
鉄	固化率	0.626	0.681
	残湯濃度(ppb-wt)	23	14
	結晶トップ濃度(atoms/cm <sup>3</sup> )	$2 \times 10^9$	$0.9 \times 10^9$
	固化率0.6濃度(atoms/cm <sup>3</sup> )	$5 \times 10^9$	$2.2 \times 10^9$
クロム	固化率	0.626	0.681
	残湯濃度(ppb-wt)	3.8	0.8
	結晶トップ濃度(atoms/cm <sup>3</sup> )	$1.1 \times 10^9$	$0.2 \times 10^9$
	固化率0.6濃度(atoms/cm <sup>3</sup> )	$2.8 \times 10^9$	$0.5 \times 10^9$
ニッケル	固化率	0.626	0.681
	残湯濃度(ppb-wt)	3.8	0.8
	結晶トップ濃度(atoms/cm <sup>3</sup> )	$1.1 \times 10^9$	$0.2 \times 10^9$
	固化率0.6濃度(atoms/cm <sup>3</sup> )	$2.8 \times 10^9$	$0.5 \times 10^9$

【0023】表1の予察から明らかなように、鉄、クロム及びニッケルの各元素の濃度がリメルトにより減少することが判った。予察に用いた塊状の多結晶シリコンをポリエチレン製のかご内に入れ、このかごを第1槽内に置いて噴射ノズルからオゾン濃度が20 ppmの溶存オゾン水溶液を5000cc/分の割合で多結晶シリコンに3分間噴射した。次いで第2槽に貯えられたオゾン濃度が20 ppmの溶存オゾン水溶液中に上記噴射処理された多結晶シリコンの入ったかごを5分間浸漬した。次いでこのかごを第2槽から引上げて、第3槽に貯えられた濃度が0.5重量%のフッ酸中に5分間浸漬した。次いでこのかごを第3槽から引上げて、第4槽内に置き、噴射ノズルからオゾン濃度が20 ppmの溶存オゾン水溶液を5000cc/分の割合で多結晶シリコンに3分間噴射した。次いでこのかごを第4槽から引上げて、第5槽に貯えられた濃度が0.5重量%のフッ酸中に5分間浸漬した。次いでこのかごを第5槽から引上げて、第6槽に貯えられた超純水中に15分間浸漬した。次いでこのかごを第6槽から引上げて、温風乾燥機内に導入し、多結晶シリコンを乾燥した後、乾燥した多結晶シリコンをかごから取出した。この洗浄後の多結晶シリコンの鉄元素濃度をICP質量分析計で測定したところ、平均値が1ppb-wtであった。

【0024】洗浄した多結晶シリコン110kgを石英るつばに入れ、カーボンヒータにより融解してシリコン融液にした。種結晶をシリコン融液に接触し、シリコン単結晶インゴットを育成した。引上げたインゴットを測定したところ、重量は80kg(固化率0.73)、引

上げ長は1100mmであった。引上げたインゴットを破碎機で塊状に破碎した。この塊状の単結晶シリコンをポリエチレン製のかご内に入れ、このかごを第7槽に貯えられたアセトン中に30分間浸漬した。次いでこのかごを第7槽から引上げて、第8槽に貯えられた濃度が50重量%のフッ酸と70重量%の硝酸の混合溶液中に5分間浸漬した。次いでこのかごを第8槽から引上げて、第9槽に貯えられた超純水中に15分間浸漬した。次いでこのかごを第9槽から引上げて、第8槽(混酸、5分) - 第9槽(超純水、15分) - 第8槽(混酸、5分) - 第9槽(超純水、15分)への浸漬を行った。かごを第9槽から引上げ、温風乾燥機内に導入し、単結晶シリコンを乾燥した後、乾燥した単結晶シリコンをかごから取出した。この洗浄後の単結晶シリコンの鉄元素濃度をICP質量分析計で測定したところ、0.05ppb-wt以下であった。

【0025】洗浄した単結晶シリコン110kgを石英るつばに入れ、カーボンヒータにより再度融解(リメルト)してシリコン融液にした。種結晶をシリコン融液に接触し、シリコン単結晶インゴットを育成した。ここでは図4に示した位置P<sub>1</sub>に対応する領域をインゴット全長にわたって育成するようにV/Gを定めて引上げた。引上げたインゴットを測定したところ、重量は80kg(固化率0.73)、引上げ長は1100mmであった。こうして引上げられたインゴットからスライスされたシリコンウェーハをラッピングし、面取り加工を施した後、鏡面研磨することにより、シリコンウェーハを得た。得られたシリコンウェーハをSPV(surface phot

$\circ$  voltage) 法により鉄元素濃度を測定したところ、平均値が約  $1 \times 10^9$  atoms/cm<sup>3</sup> であった。

【0026】また上記シリコンウェーハの結晶欠陥であるCOP、OSF及びL/Dについて測定した。COPは、シリコンウェーハをアンモニアと過酸化水素の混合液で洗浄した後、レーザパーティクルカウンタ (KLA-Tencor社製、SFS6200) を用いて、このウェーハの表面における0.12 μm以上のサイズのCOPを調べた。またOSFは、シリコンウェーハを100°Cの温度で4時間熱処理し、引き続き1130°Cの温度で3時間熱処理(バイロジエニック酸化処理)して、目視によりOSFが顕在化しているか否か調べた。更にL/Dは、上記シリコンウェーハ表面を30分間セコ(Secco)エッティング液で化学エッティングした。次いでこれにより現れる特異な痕跡を光学顕微鏡で観察し、基板であるシリコンウェーハのL/Dの転写痕の有無を調べた。その結果、ウェーハ全面において0.12 μm以上のサイズのCOPは0個であった。またウェーハ面内でOSFもL/Dも全く出現しなかった。

#### 【0027】

【発明の効果】以上述べたように、本発明のシリコン単結晶インゴット及びこれから作られたシリコンウェーハは、結晶に起因した欠陥がなく、かつ鉄をはじめとしてクロム、ニッケルのような金属元素の汚染度が小さく電気的特性に優れている。この結果、LSI等の半導体装\*

\* 置にしたときに、pn接合においてリーク電流が少なく、またMOSトランジスタのゲート酸化膜に対する信頼性が高い。

#### 【図面の簡単な説明】

【図1】ボロンコフの理論を基づいた、V/G比が臨界点以上では空孔豊富インゴットが形成され、V/G比が臨界点以下では格子間シリコン豊富インゴットが形成されることを示す図。

【図2】所望の引上げ速度プロファイルを決定するための引上げ速度の変化を示す特性図。

【図3】本発明による空孔豊富ウェーハ及びバーフェクトウェーハをそれぞれ成長させるための引上げ速度プロファイルを図式的に示した特性図。

【図4】本発明による基準インゴットの空孔豊富領域、格子間シリコン豊富領域及びバーフェクト領域を示すX線トモグラフィの概略図。

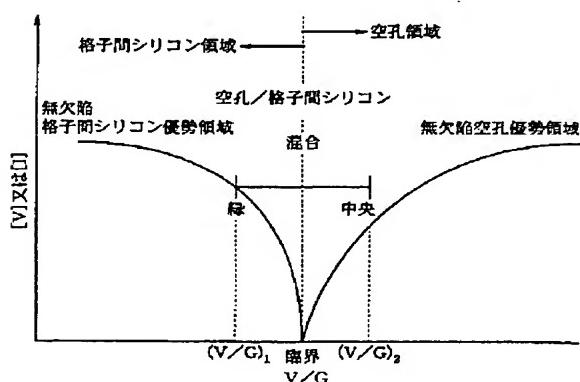
【図5】本発明の空孔型点欠陥の凝集体及び格子間シリコン型点欠陥の凝集体が存在しないインゴット及びウェーハの説明図。

【図6】そのウェーハの平面図。

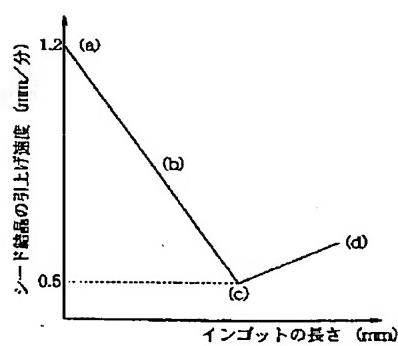
【図7】中央に空孔豊富領域と、この空孔豊富領域とウェーハの縁部分の間の無欠陥領域を有するインゴット及びウェーハの説明図。

【図8】そのウェーハの平面図。

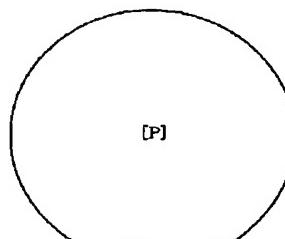
【図1】



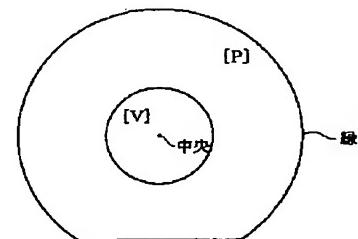
【図2】



【図6】

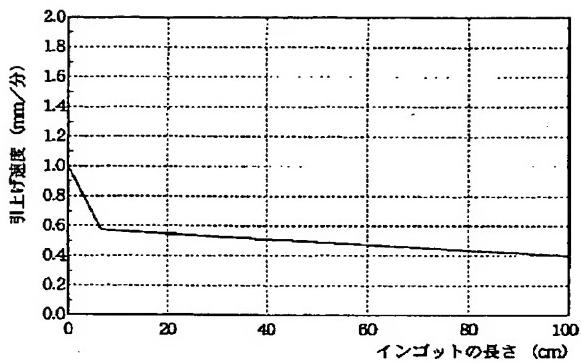


中心

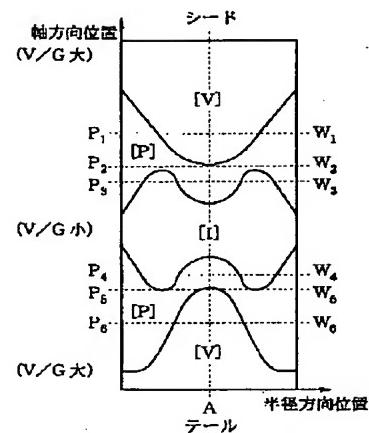


【図8】

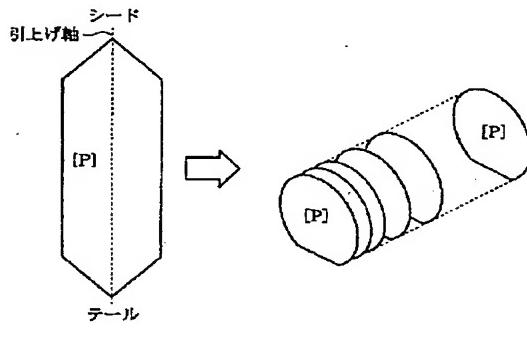
【図3】



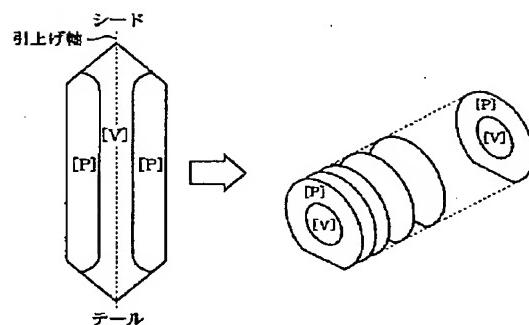
【図4】



【図5】



【図7】



フロントページの続き

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**(21)Application number :** 11-146055**(71)Applicant :** MITSUBISHI MATERIALS SILICON CORP  
MITSUBISHI MATERIALS CORP**(22)Date of filing :** 26.05.1999**(72)Inventor :** HARADA KAZUHIRO  
FURUYA HISASHI

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**(54) SILICON SINGLE CRYSTAL INGOT AND SILICON WAFER MADE OF THE SAME****(57)Abstract:**

**PROBLEM TO BE SOLVED:** To obtain a single crystal ingot and wafer excellent in electrical characteristics by suppressing the formation of agglomerate of hole-type point defects and interstitial silicon-type point defects and lowering the contamination concentration of iron to be not more than a specific value in a Czochralski method.

**SOLUTION:** Silicon molten liquid is obtained by washing, preferably at least two times, source silicon with an aqueous solution containing dissolved ozone and then hydrofluoric acid or nitrohydrofluoric acid, and, after finally washing with ultra-pure water, melting the source silicon in a furnace based on a Czochralski method. The ratio of solidification is preferably set to be not less than 0.9 at initial pulling-up and the ratio of solidification is set to be not more than 0.9, preferably not more than 0.8 when the single crystal is pulled up after remelting. Thereby, the contamination concentration of iron element becomes not more than  $2 \times 10^9$  atoms/cm<sup>3</sup>. When the rate of pulling-up an ingot is set as V (mm/min) and the temp. gradient at the interface between the ingot and the silicon molten liquid is set to be G( $^{\circ}$ C/mm), the value of V/G (mm<sup>2</sup>/min. $^{\circ}$ C) is determined over whole length of the ingot by simulation, and the ingot is grown, thereby a crystal free from defects can be obtained.

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**LEGAL STATUS****[Date of request for examination]** 22.08.2002**[Date of sending the examiner's decision of rejection]** 13.09.2005**[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]****[Date of final disposal for application]****[Patent number]****[Date of registration]****[Number of appeal against examiner's decision of rejection]** 2005-19373**[Date of requesting appeal against examiner's decision of rejection]** 06.10.2005**[Date of extinction of right]**

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**CLAIMS**

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**[Claim(s)]**

[Claim 1] The silicon single crystal ingot characterized by being the silicon single crystal ingot raised by the Czochralski method with which the floc of a hole mold point defect and the floc of the silicon mold point defect between grids do not exist, and iron concentration of contamination being three or less  $2 \times 10^9$  atoms/cm.

[Claim 2] The silicon wafer made from the silicon single crystal ingot according to claim 1.

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## DETAILED DESCRIPTION

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### [Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the silicon wafer made the silicon single crystal ingot raised by the Czochralski method (henceforth a CZ process), and from now on. Furthermore, it is related with the silicon wafer used in detail in order to manufacture semiconductor devices, such as LSI.

[0002]

[Description of the Prior Art] It is required that the electrical characteristics which were [ be / semiconductor devices, such as LSI, have little leakage current in pn junction, and / the dependability over the gate oxide of an MOS transistor / high ] excellent should be shown. As a cause of degrading these properties, contamination by the crystal defect of the silicon wafer used as a substrate and the metallic element of a wafer is cited. Especially the iron element is supposed that a bad influence is done strongly in the silicon single crystal also in the metal, and this iron element is incorporated by contamination from a surrounding environment or equipment.

[0003] The in thorin chic (gettering IG) law and extrinsic gettering (EG) method for giving the gettering capacity to capture a metallic element, from the former to the wafer itself as a technique of capturing a metallic element like an iron element from the active region of this silicon wafer is learned. Moreover, after SC-1 solution which consists of a hydrogen peroxide and ammonium hydroxide washes a silicon wafer as a technique of removing a metal from the wafer front face used as an active region, the RCA cleaning method washed with SC-2 solution which consists of a hydrogen peroxide and dilute hydrochloric acid is known.

[0004]

[Problem(s) to be Solved by the Invention] However, if many metallic elements are mixed in the silicon single crystal ingot raised by the CZ process, the technique of removing or capturing the metallic element in the condition of a silicon wafer must be complicated or developed increasingly. The purpose of this invention does not have a defect resulting from a crystal, and the degree of contamination of a metallic element like an iron element is to offer the silicon wafer made a silicon single crystal ingot and from now on was small excellent in electrical characteristics.

[0005]

[Means for Solving the Problem] Invention concerning claim 1 is a silicon single crystal ingot in which the floc of the hole mold point defect raised by the Czochralski method and the floc of the silicon point defect between grids do not exist, and is a silicon single crystal ingot characterized by iron concentration of contamination being three or less  $2 \times 10^9$  atoms/cm. Invention concerning claim 2 is the silicon wafer made from the silicon single crystal ingot according to claim 1. Since iron concentration of contamination is as low as three or less  $2 \times 10^9$  atoms/cm, when the silicon wafer concerning the ingot concerning claim 1 or claim 2 did not have a defect resulting from a crystal, and it is made semiconductor devices, such as LSI, the electrical characteristics which were [ be / there is little leakage current in pn junction, and / the dependability over the gate oxide of an MOS transistor / high ] excellent are shown.

[0006]

[Embodiment of the Invention] How to lessen the content of a metallic element, and for it to be defect-free and to manufacture the silicon single crystal ingot of this invention is described.

(1) The silicon single crystal ingot with few contents of the metallic element of manufacture approach this invention of a silicon single crystal with few contents of a metallic element, especially an iron element. The process which washes the massive or granular polycrystalline silicon used as a raw material, and the pull-up process of a silicon single crystal of dissolving the washed raw material silicon and raising a silicon single crystal ingot at 0.9 or less rate of solidification by the CZ process from this silicon melt, The process which makes this silicon single crystal pulled up massive or granular, the process which washes this massive or granular single crystal silicon, and the re-pull-up process of the silicon single crystal which dissolves the washed silicon single crystal again (RIMERUTO), and is raised at 0.9 or less rate of solidification are included. The rate of solidification means the rate of the silicon single crystal raised to raw material silicon 100% by weight conversion here.

[0007] In order to wash the polycrystalline silicon or the single crystal silicon used as raw material silicon, after a dissolved ozone water solution washes massive or granular raw material silicon first, it is the approach of washing with fluoric acid or a FUTSU nitric acid (mixed acid of fluoric acid and a nitric acid), and washing with ultrapure water further. It is desirable to repeat the washing process by this fluoric acid or the FUTSU nitric acid once or more, or to repeat the washing process by the dissolved ozone water solution and the washing process by fluoric acid or the FUTSU nitric acid once or more. It is put in and sealed by the bag made from plastics until it feeds it into a quartz crucible, since raw material silicon, such as polycrystalline silicon or single crystal silicon, has an activity property. However, it reacts with the oxygen in air before and after seal, and an oxide film is easy to be formed in the front face of raw material silicon. This oxide film is formed including the metal impurity adhering to the front face of raw material silicon etc., or a metal impurity etc. adheres on the surface of an oxide film after formation of an oxide film. In the above-mentioned approach, a silicon front face oxidizes compulsorily by washing of a dissolved ozone water solution, an oxide film is formed all over silicon, and, subsequently this oxide film is removed by washing of fluoric acid or a FUTSU nitric acid. Consequently, the metal impurity contained in an oxide film is removed with an oxide film. The removal effectiveness increases by repeating the washing process by fluoric acid or the FUTSU nitric acid once or more.

[0008] The raw material silicon obtained by the above-mentioned washing is dissolved at the furnace based on a CZ process, and serves as silicon melt. The rate of solidification at the time of the first pull-up is set or more to 0.9, and the rate of solidification at the time of the pull-up after RIMERUTO is preferably set or less to 0.8 0.9 or less here. Making the rate of solidification below into the above-mentioned value is based on the following reason. The rate of solidification is small and the part in which it was raised when the silicon melt in a quartz crucible remained so much, i.e., the part near the top section of an ingot, has few amounts of mixing of metallic elements, such as iron in silicon melt. The concentration of the metallic element in residual liquor is to become high and for

the amount of mixing to the ingot of a metallic element to increase as the residual liquor of the silicon melt in a quartz crucible decreases and the rate of solidification becomes large on the other hand. By washing of raw material silicon, and RIMERUTO below the predetermined rate of solidification, the iron concentration of contamination in a silicon single crystal becomes three or less  $2 \times 10^9$  atoms/cm.

[0009] (2) the manufacture approach of a defect-free silicon single crystal -- describe the manufacture approach of a defect-free silicon single crystal that next the floc of a hole mold point defect and the floc of the silicon mold point defect between grids do not exist. The silicon single crystal ingot of this invention can pull up an ingot from the silicon melt in a hot zone furnace by the CZ process by the predetermined pull-up rate profile based on Voronkov's (Voronkov) theory. Moreover, the silicon wafer of this invention slices this ingot, and is produced. Generally, when the ingot of a silicon single crystal is pulled up from the silicon melt in a hot zone furnace by the CZ process, the floc (agglomerates: three-dimensions defect) of a point defect (point defect) and a point defect occurs as a defect in a silicon single crystal. A point defect has two general gestalten of a hole mold point defect and the silicon mold point defect between grids. A hole mold point defect secedes from one of the normal-[ one silicon atom / in a silicon crystal lattice ] locations. Such a hole becomes a hole mold point defect. On the other hand, if an atom is discovered in locations other than the lattice point of a silicon crystal (interstitial site), this will become a silicon point defect between grids.

[0010] Generally a point defect is formed in the contact surface between silicon melt (melting silicon) and an ingot (solid silicon). However, it is begun by pulling up an ingot continuously to cool the part which was the contact surface with a pull-up. During cooling, a hole mold point defect or the silicon mold point defect between grids joins mutually by diffusion, and the floc (vacancy agglomerates) of a hole mold point defect or the floc (interstitial agglomerates) of the silicon mold point defect between grids is formed. In other words, floc is the three-dimensional structure which originates in the union of a point defect and is generated. The floc of the silicon mold point defect between grids includes the defect called ratio of length to diameter (Interstitial-type Large Dislocation) including the defect to which the floc of a hole mold point defect is called COP (Crystal Originated Particle), LSTD (Laser Scattering Tomograph Defects), or FPD (Flow Pattern Defects). COP is a defect resulting from the crystal with which a pit is also detected as particle with original particle here, when a pit will be formed in a wafer front face if the silicon wafer after mirror polishing is washed with the mixed liquor of ammonia and a hydrogen peroxide, and this wafer is measured with a particle counter. In FPD, it is the source of the trace which presents the unique flow pattern which appears when chemical etching of the silicon wafer which sliced the ingot and was produced is carried out with the SEKÖ (Secco) etching reagent during 30 minutes, and when LSTD irradiates infrared radiation in a silicon single crystal, silicon is a source which has a different refractive index and generates the scattered light. If ratio of length to diameter is also called a rearrangement cluster or the silicon wafer which produced this defect is immersed in the selection etching reagent used as a principal component in fluoric acid, since it will produce a pit, it is also called a rearrangement pit.

[0011] When setting the temperature gradient of the contact surface of ingot-silicon melt to G (degree C/mm) for the pull-up rate of an ingot with V (a part for mm/), and hot zone structure, Voronkov's theory is controlling V/G (a part for  $2/[ \text{mm} ]^{-**}$ ), in order to grow up a high grade ingot with few defects. In this theory, as shown in drawing 1, V/G expresses hole concentration and the silicon concentration between grids in graph as a function, and it explains that the boundary of a hole / silicon field between grids is determined by V/G with a wafer. While the ingot in which a hole mold point defect exists [ a V/G ratio ] dominantly above the critical point is formed in more detail, the ingot in which the silicon mold point defect between grids exists [ a V/G ratio ] dominantly below in the critical point is formed.

[0012] When an ingot can pull up the predetermined pull-up rate profile of this invention from the silicon melt in a hot zone furnace, It is more than the 1st critical ratio ( $v/G$ ) (1) to which the ratio ( $V/G$ ) of a pull-up rate to a temperature gradient prevents generating of the floc of the silicon mold point defect between grids. It is decided that it is maintained below at the 2nd critical ratio ( $V/G$ ) (2) which restricts the floc of a hole mold point defect in the field where the hole mold point defect which exists in the center of an ingot exists dominantly. The profile of this pull-up rate is slicing a criteria ingot to shaft orientations experimentally, and is slicing a criteria ingot to a wafer experimentally, or is combining these techniques, and is determined by simulation based on above-mentioned Voronkov's theory. That is, this decision checks after simulation the wafer with which the ingot was sliced [ with which were sliced and it was shaft-orientations-sliced ], and is made by repeating simulation further. Two or more kinds of pull-up rates are decided in the predetermined range for simulation, and two or more criteria ingots grow. As shown in drawing 2  $R > 2$ , the pull-up rate profile for simulation is adjusted to low 0.5mm pull-up rate for /c), and an again high pull-up rate (d) from a high 1.2mm pull-up rate (a) like [ for /]. the above -- a low pull-up rate may be less than [ 0.4mm a part for /and it ], and its linearity-thing is [ the change by the pull-up rate (b) and (d) ] desirable.

[0013] It can pull up at a different rate and two or more criteria ingots are sliced by shaft orientations at each \*\*. Optimal V/G is determined from the slice of shaft orientations, the check of a wafer, and the correlation as a result of simulation, the optimal pull-up rate profile is continuously determined, and an ingot is manufactured by the profile. An actual pull-up rate profile is dependent on many variables which are not limited to the ability of the diameter of a desired ingot, the specific hot zone furnace used, the quality of silicon melt, etc. to be included.

[0014] Drawing 3 shows the profile of the pull-up rate for growing up the ingot which has die length of 100cm and the diameter of 200mm which were determined using simulation and association of an experimental technique. Here, the hot zone furnace based on the CZ process of the model name Q41 manufactured at MITSUBISHI MATERIALS silicon Ikuno works was used.

[0015] A pull-up rate is reduced gradually, V/G is reduced continuously, and when the sectional view of the ingot when raising a pull-up rate gradually again and raising V/G continuously is drawn, the fact shown in drawing 4 is known. The perfect field where the floc of [ ] and a hole mold point defect and the floc of the silicon mold point defect between grids do not exist [ the field where the silicon mold point defect between [V] grids exists / the field where the hole mold point defect within an ingot exists dominantly / in drawing 4 dominantly ] is shown as [P], respectively. As shown in drawing 4, the shaft-orientations locations P1 and P6 of an ingot include the field where a hole mold point defect exists in the center dominantly. Locations P3 and P4 include the perfect field of the ring with which the silicon mold point defect between grids exists dominantly, and a center. Moreover, since there is no hole mold point defect in the center and a part for a edge does not have a silicon mold point defect between grids, either, locations P2 and P5 are perfect fields altogether.

[0016] The wafers W1 and W6 corresponding to two or more locations P1 and P6 include the field where a hole mold point defect exists in the center dominantly, respectively so that clearly from drawing 4. Wafer W3 and W4 include the perfect field of the ring with which the silicon mold point defect between grids exists dominantly, and a center. Moreover, since there is no hole mold point defect in the center and a part for a edge does not have a silicon mold point defect between grids, either, wafers W2 and W5 are perfect fields altogether. Wafers W2 and W5 slice the ingot which selected and was decided to make a perfect field altogether as shown in drawing 5 and which pulled up and grew by the rate profile, and are produced. Drawing 6 is the top view. The wafers W1 and W6 which sliced the ingot which grew by another pull-up rate profile, and were produced by reference are shown in drawing 7. Drawing 8

is the top view. The silicon wafer of this invention is the above-mentioned wafer W2 or W5, and after wrapping this wafer and performing beveling processing, mirror polishing of it is carried out and it is obtained.

[0017]

[Example] Next, the example of this invention is explained. When the iron element concentration of the polycrystalline silicon used as a raw material was measured with the ICP mass spectrometer (inductively coupled plasma mass spectrometer), the average was 2 ppb-wt. That the concentration of an iron element is 2 ppb-wt means that iron is contained at a rate of 2ppb to silicon 1g. Generally, the high impurity concentration in a silicon single crystal is extremely small because of a segregation, and carrying out the direct method of analysis has many difficult elements. Then, after raising a single crystal by the CZ process, the silicon melt (henceforth residual molten iron) which remained in the crucible is analyzed, and the approach of computing the high impurity concentration under crystal is taken from the segregation coefficient of each impurity element. This analysis dissolves this sample whole quantity with the mixed acid of high grade fluoric acid and a nitric acid, after usually sampling a part of residual molten iron and making it solidify, and it analyzes it with an ICP mass spectrometer.

[0018] In this example, the RIMERUTO trial of residual-molten-iron analysis of silicon melt and a silicon single crystal which dissolved polycrystalline silicon beforehand was performed, and the concentration of iron, chromium, and nickel was considered among metal impurities. That is, the single crystal was pulled up from the silicon melt which dissolved the above-mentioned polycrystalline silicon to die length of 220mm. The residual molten iron at the time of the rate 0.626 of solidification was sampled, it solidified, and the concentration of each element of iron, chromium, and nickel was measured. Moreover, the concentration of each element of the iron of the top section of a single crystal, chromium, and nickel was also measured. Subsequently, the raised silicon single crystal was dissolved again (RIMERUTO), and the single crystal was too pulled up from this silicon melt to die length of 220mm. The residual molten iron at the time of the rate 0.681 of solidification was sampled, it solidified, and the concentration of each element of iron, chromium, and nickel was measured. Moreover, the concentration of each element of the iron of the top section of a single crystal, chromium, and nickel was also measured.

[0019] The high impurity concentration of the top section of each single crystal pulled up from the silicon melt and the silicon melt dissolved again of the above-mentioned beginning assumed that all impurities were mixing into silicon melt before crystal training, and was calculated using the following formula (1).

[0020]

[Equation 1]

$$C_T = \frac{k_0 C_z}{(1 - L)^{k_0-1}} \quad \dots \quad (1)$$

[0021] However, for CT, the high impurity concentration of the top section and k0 are [ the high impurity concentration in residual molten iron and L of a segregation coefficient and CZ ] the rates of solidification at the time of residual-molten-iron analysis. The segregation coefficient of an iron element is [ the segregation coefficient of  $2.8 \times 10^{-5}$  and a nickel element of the segregation coefficient of  $8 \times 10^{-6}$  and a chromium element ]  $3 \times 10^{-5}$ . Results, such as high impurity concentration in residual molten iron and high impurity concentration of the top section, are shown in Table 1.

[0022]

[Table 1]

		多結晶シリコン	単結晶リメルト (固化率0.9以下)
鉄	固化率	0.626	0.681
	残湯濃度(ppb-wt)	23	14
	結晶トップ濃度(atoms/cm³)	$2 \times 10^9$	$0.9 \times 10^9$
	固化率0.6濃度(atoms/cm³)	$5 \times 10^9$	$2.2 \times 10^9$
クロム	固化率	0.626	0.681
	残湯濃度(ppb-wt)	3.8	0.8
	結晶トップ濃度(atoms/cm³)	$1.1 \times 10^9$	$0.2 \times 10^9$
	固化率0.6濃度(atoms/cm³)	$2.8 \times 10^9$	$0.5 \times 10^9$
ニッケル	固化率	0.626	0.681
	残湯濃度(ppb-wt)	3.8	0.8
	結晶トップ濃度(atoms/cm³)	$1.1 \times 10^9$	$0.2 \times 10^9$
	固化率0.6濃度(atoms/cm³)	$2.8 \times 10^9$	$0.5 \times 10^9$

[0023] It turned out that the concentration of each element of iron, chromium, and nickel decreases by RIMERUTO so that clearly from the prediction of Table 1. The massive polycrystalline silicon used for prediction was put in in the cage made from polyethylene,

this cage was placed into the 1st tub and the dissolved ozone water solution whose ozone level is 20 ppm was injected from the injection nozzle for 3 minutes to polycrystalline silicon at 5000 cc a rate for /. Subsequently, the ozone level stored in the 2nd tub was immersed for 5 minutes in the cage with which the polycrystalline silicon by which injection processing was carried out [ above-mentioned ] entered into the dissolved ozone water solution which is 20 ppm. Subsequently, this cage was pulled up from the 2nd tub, and it was immersed for 5 minutes into the fluoric acid whose concentration stored in the 3rd tub is 0.5 % of the weight. Subsequently, this cage was pulled up from the 3rd tub, it placed into the 4th tub, and the dissolved ozone water solution whose ozone level is 20 ppm was injected from the injection nozzle for 3 minutes to polycrystalline silicon at 5000 cc a rate for /. Subsequently, this cage was pulled up from the 4th tub, and it was immersed for 5 minutes into the fluoric acid whose concentration stored in the 5th tub is 0.5 % of the weight. Subsequently, this cage was pulled up from the 5th tub, and it was immersed for 15 minutes into the ultrapure water stored in the 6th tub. Subsequently, after having pulled up this cage from the 6th tub, introducing in the warm air dryer and drying polycrystalline silicon, the dry polycrystalline silicon was picked out from the cage. When the iron element concentration of the polycrystalline silicon after this washing was measured with the ICP mass spectrometer, the average was 1 ppb-wt.

[0024] 110kg of washed polycrystalline silicon was put into the quartz crucible, and it dissolved at the carbon heater, and was made silicon melt. Silicon melt was contacted in seed crystal and the silicon single crystal ingot was raised. When the ingot pulled up was measured, weight was 80kg (rate 0.73 of solidification), and pull-up length was 1100mm. The ingot pulled up was crushed massive by the crusher. This massive single crystal silicon was put in in the cage made from polyethylene, and it was immersed for 30 minutes into the acetone stored in the 7th tub in this cage. Subsequently, this cage was pulled up from the 7th tub, and it was immersed for 5 minutes into the mixed solution of the fluoric acid whose concentration stored in the 8th tub is 50 % of the weight, and 70% of the weight of a nitric acid. Subsequently, this cage was pulled up from the 8th tub, and it was immersed for 15 minutes into the ultrapure water stored in the 9th tub. Subsequently, this cage was pulled up from the 9th tub, and immersion to the 8th tub (mixed-acid, 5 minutes)-9th tub (ultrapure water, 15 minutes)-8th tub (mixed-acid, 5 minutes)-9th tub (ultrapure water, 15 minutes) was performed. After having pulled up the cage from the 9th tub, introducing in the warm air dryer and drying single crystal silicon, the dry single crystal silicon was picked out from the cage. When the iron element concentration of the single crystal silicon after this washing was measured with the ICP mass spectrometer, they were 0.05 or less ppb-wt.

[0025] 110kg of washed single crystal silicon was put into the quartz crucible, and it dissolved again at the carbon heater (RIMERUTO), and was made silicon melt. Silicon melt was contacted in seed crystal and the silicon single crystal ingot was raised. Here, V/G was defined and pulled up so that the field corresponding to the location P2 shown in drawing 4 might be raised covering an ingot overall length. When the ingot pulled up was measured, weight was 80kg (rate 0.73 of solidification), and pull-up length was 1100mm. In this way, after wrapping the silicon wafer sliced from the ingot which was able to be pulled up and performing beveling processing, the silicon wafer was obtained by carrying out mirror polishing. the obtained silicon wafer -- SPV (surface photo voltage) -- the place which measured iron element concentration by law -- the average -- about -- it was  $1 \times 10^9$  atoms/cm<sup>3</sup>.

[0026] Moreover, it measured about COP, OSF, and ratio of length to diameter which are the crystal defect of the above-mentioned silicon wafer. COP investigated COP with a size [ in the front face of this wafer ] of 0.12 micrometers or more using the laser particle counter (the product made from KLA-Tencor, SFS6200), after washing the silicon wafer with the mixed liquor of ammonia and a hydrogen peroxide. Moreover, OSF investigated whether a silicon wafer would be heat-treated at the temperature of 1000 degrees C for 4 hours, heat treatment (pie ROJIE nick oxidation treatment) would be successively carried out at the temperature of 1130 degrees C for 3 hours, and OSF would actualize by viewing. Furthermore, ratio of length to diameter carried out chemical etching of the above-mentioned silicon wafer front face with the SEKO (Secco) etching reagent during 30 minutes. Subsequently, the unique trace which appears by this was observed with the optical microscope, and the existence of the imprint marks of ratio of length to diameter of the silicon wafer which is a substrate was investigated. Consequently, on the whole wafer surface, the number of COP with a size of 0.12 micrometers or more was zero. Moreover, OSF or ratio of length to diameter did not appear at all in the wafer side.

[0027]

[Effect of the Invention] As stated above, the silicon wafer made the silicon single crystal ingot of this invention and from now on does not have a defect resulting from a crystal, and the degree of contamination of a metallic element like chromium including iron and nickel is small excellent in electrical characteristics. Consequently, when it is made semiconductor devices, such as LSI, there is little leakage current in pn junction, and the dependability over the gate oxide of an MOS transistor is high.

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[Translation done.]

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## DESCRIPTION OF DRAWINGS

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### [Brief Description of the Drawings]

[Drawing 1] Drawing in which a hole abundance ingot is formed in for the V/G ratio based in Voronkov's theory above the critical point, and a V/G ratio shows that the silicon abundance ingot between grids is formed below in the critical point.

[Drawing 2] The property Fig. showing change of the pull-up rate for determining a desired pull-up rate profile.

[Drawing 3] The property Fig. having shown the pull-up rate profile for growing up the hole abundance wafer and perfect wafer by this invention, respectively in graph.

[Drawing 4] The schematic diagram of X-ray tomography showing the hole abundance field of the criteria ingot by this invention, the silicon abundance field between grids, and a perfect field.

[Drawing 5] The ingot in which the floc of the hole mold point defect of this invention and the floc of the silicon mold point defect between grids do not exist, and the explanatory view of a wafer.

[Drawing 6] The top view of the wafer.

[Drawing 7] The ingot which has a hole abundance field, and this hole abundance field and the defect-free field of the between for a edge [ wafer ] in the center, and the explanatory view of a wafer.

[Drawing 8] The top view of the wafer.

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[Translation done.]

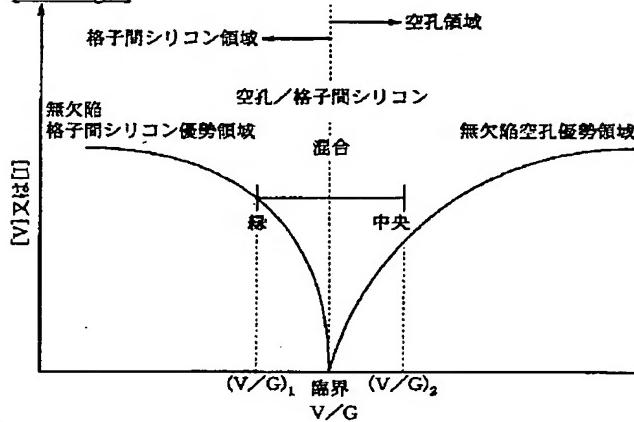
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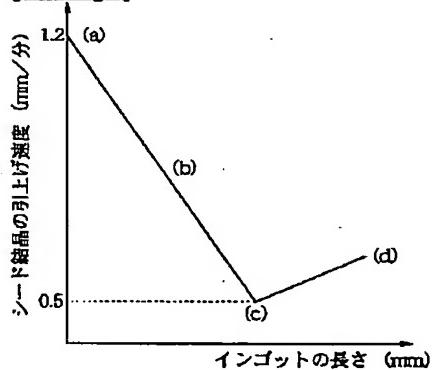
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## DRAWINGS

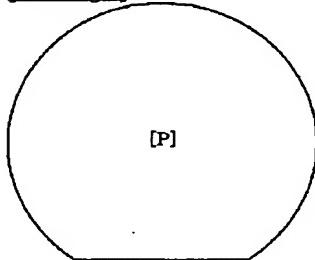
[Drawing 1]



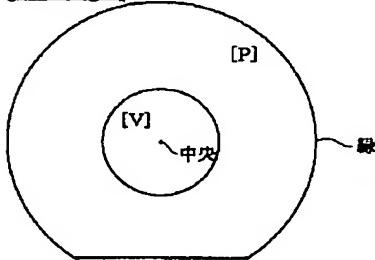
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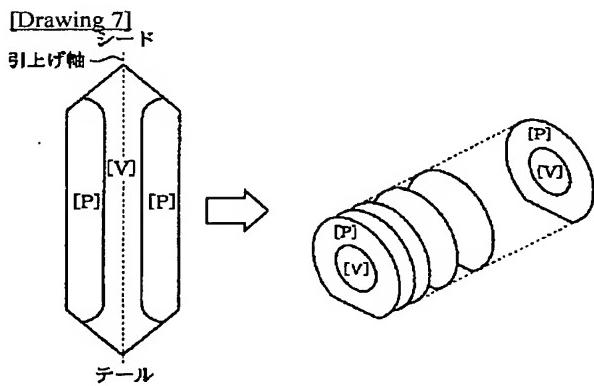
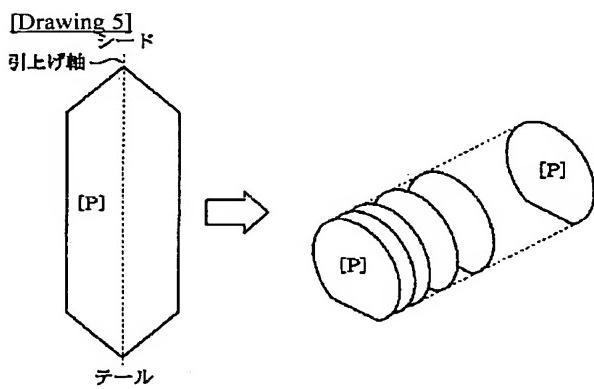
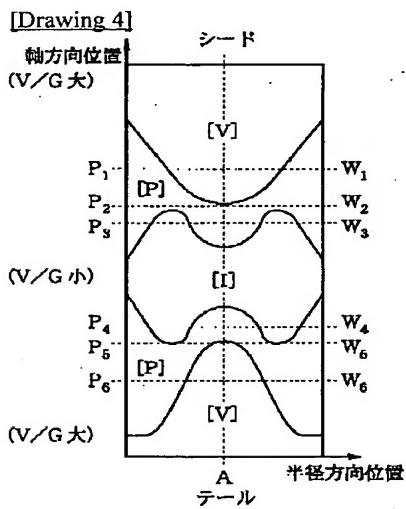
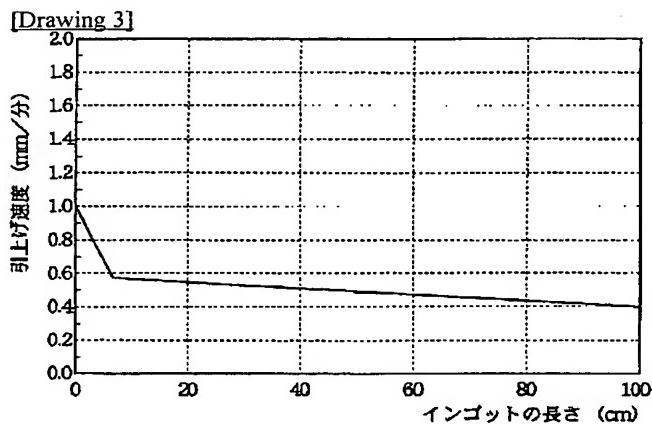


[Drawing 6]



[Drawing 8]





[Translation done.]

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